A 0.02-to-6GHz SDR Balun-LNA Using a Triple-Stage Inverter-Based Amplifier

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***Abstract*—This paper describes a software-defined-radio (SDR) balun low-noise amplifier (LNA) with no explicit bias circuit, inductor or ac-coupling network. It relies on a triple-stage inverter-based amplifier with resistive feedback to maximize the bandwidth and realize single-to-differential conversion. *RC* degeneration applied at the last gain stage enhances both linearity and output gain-phase balancing. Optimized in 65-nm CMOS the balun-LNA covers the 0.02-to-6-GHz band with S_{11}<–11 dB, voltage gain of 21.2-dB and noise figure below 3.2-dB. The in-band IIP2 (IIP3) is +36 to +51 dBm (–5.6 to –5.3 dBm). The power consumption is 7.9 mW at 1.2 V.**

I. Introduction

The global development of diverse wireless standards to enable seamless connectivity all over the world calls for software-defined-radio (SDR) wireless solutions [1]. The rapid down-scaling of CMOS allows the emergence of more compact and faster RF circuits capable of supporting all essential bands up to 6 GHz or beyond. An inductorless SDR balun low-noise amplifier (LNA) is attractive to avoid the need of multiple off-chip baluns while maximizing the hardware reuse in expensive nm-length CMOS technologies.

The sensitivity, intermodulation distortion and output gain-phase balancing are the three main receiver parameters determining the balun-LNA specifications. The sensitivity is mainly limited by the noise figure (NF) of the balun-LNA. The intermodulation distortion determines the capability of a receiver in preventing intermodulation products from corrupting the desired channel. In narrowband receivers with differential implementation, the 3rd-order inter-modulation product is the main component to be considered. However, in wideband SDR receivers, both the 2nd-order and 3rd-order intermodulation products might fall into the IF frequency, corrupting the desired channel [2, 3]. The output gain-phase balancing ensures that the RF signal is balanced before it is fed into the mixers to secure the advantages of differential implementation.

The SDR balun-LNA proposed here will adopt a resistive-feedback technique on a triple-stage inverter-based amplifier, such that adequate gain peaking can be obtained without involving any bulky inductor [4], bias current or ac-coupling network. The linearity and output gain-phase balancing are optimized via resistive-capacitive (*RC*) degeneration in the final gain stage of the balun-LNA.

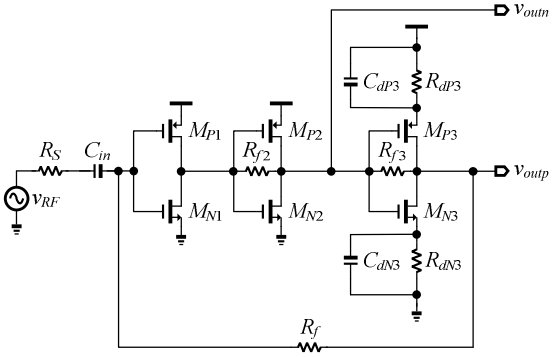

Fig. 1. Proposed SDR Balun-LNA using triple-stage inverter-based amplifier.

The proposed balun-LNA is presented in Section II. In Section III, the most significant LNA parameters are determined analytically. Section IV exhibits the simulation results to attest the LNA expected performances. Finally, in section V, the conclusions are drawn.

II. Proposed SDR Balun-LNA

The proposed SDR balun-LNA is depicted in Fig. 1. It is based on three inverter amplifiers in cascade to provide a large open loop gain, which together with the feedback resistor R_f offers the input impedance matching. A differential output is naturally available via taking the outputs of the second and third gain stages. All gain stages feature current-reuse between the NMOS and PMOS devices, doubling the stage trans-conductance for the same power. The DC operating points of the second and the third stages are ensured via their local resistive feedback, while in the first stage it will be determined by the global resistive feedback. Thus, no explicit bias circuit is entailed.

The first stage has the highest gain, since it does not have local feedback. This benefits the open loop gain and the noise figure (NF), since it reduces the noise influence of the remaining stages. The second gain stage also contributes significantly to the open-loop gain. Finally, the third stage should have ideally unity gain to enhance the output gain-phase balancing. The resistive-capacitor (*RC*) degeneration reduces the stage gain at low frequency, while maintaining the gain at high frequencies (equivalent to gain peaking to boost the bandwidth). A detailed circuit analysis is performed next.

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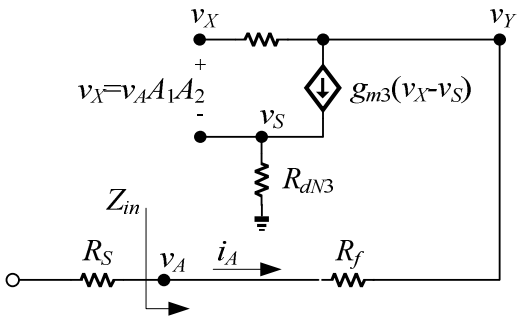

Fig. 2. The balun-LNA's small signal model for the determination of close loop voltage gain and input impedance.

III. Circuit Analysis of the Proposed Balun-LNA

The key characteristics of this balun-LNA are the input impedance, voltage gain and NF. In order to simplify the analysis the effect of the transistor's parasitic capacitances is omitted. The voltage gains of the first, second and third stages (respectively A_1, A_2 and A_3) are given by,

$$\begin{cases} A_1 \approx -(g_{mN1}+g_{mP1})r_{o1} \,//\, R_{f2} \\ A_2 \approx -\left(g_{mN2}+g_{mP2}-\dfrac{1}{R_{f2}}\right)R_{f2} \,//\, R_{f3} \,//\, r_{o2} \\ A_3 \approx -\left(\dfrac{g_{mN3}}{1+g_{mN3}Z_{dN3}}+\dfrac{g_{mP3}}{1+g_{mP3}Z_{dP3}}-\dfrac{1}{R_{f3}}\right)R_{f3} \,//\, R_f \,//\, r_{o3} \\ r_{o1}=r_{oN1} \,//\, r_{oP1},\ r_{o2}=r_{oN2} \,//\, r_{oP2},\ r_{o3}=r_{oN3} \,//\, r_{oP3} \\ Z_{dN3}=R_{dN3}+\dfrac{1}{sC_{dN3}},\ Z_{dP3}=R_{dP3}+\dfrac{1}{sC_{dP3}} \end{cases} \quad (1)$$

The gain of the first stage is mainly determined by its transconductance and by the local feedback resistance of the second stage in parallel with r_o of the transistors that for recent technologies might be of the same order, which prevents them from being neglected. The gain of this stage should be maximized, to minimize the noise influence of the following stages. Increasing the transconductance increases the power consumption; thus, at a first glance, it seems better to increase R_{f2}; which also increases the second stage gain. However, a high R_{f2} penalizes linearity, due to the gain increase, meaning that a compromise between both variables should be met. The gain of the third stage, that must be equal to –1, can be controlled by at least four variables: the transistors trans-conductance, the degeneration resistors, the degeneration capacitors, and the local feedback resistor R_{f3}. They should be sized considering their influence on the power consumption, the gain, and the output gain and phase imbalance.

The overall voltage gain, A_v, and the input impedance Z_{in} are determined by the circuit represented in Fig. 2, and are given by eqs. (2) and (3), respectively,

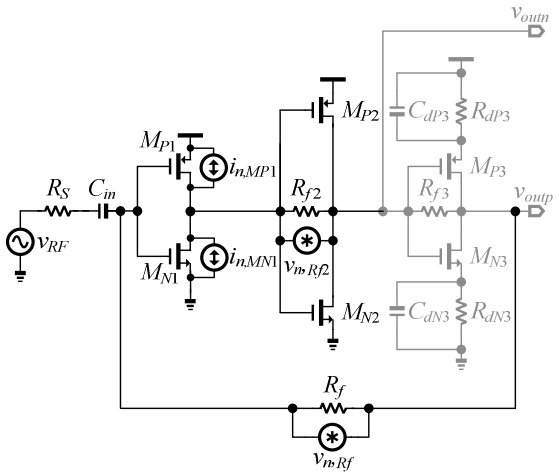

Fig. 3. Balun-LNA with critical noise sources added for noise analysis.

$$A_v = \frac{v_X - v_Y}{v_A} = A_1 A_2 (1 - A_3) \quad (2)$$

$$Z_{in} = \frac{v_A}{i_A} = \frac{Rf}{1 - A_1 A_2 A_3} \quad (3)$$

where $v_Y = A_3 v_X \approx -1 v_X$, $v_X = A_1 A_2 v_A$, and $v_A = i_A R_f + v_Y$. The voltage gain is mainly dominated by the gain of the first stage. The input impedance is mainly determined by the feedback resistance and the cascaded gain. Increasing both variables, while keeping the input impedance matching, benefits the overall gain and NF. Again, the trade-off here is the power consumption.

To determine the NF, we consider the next four noise sources, as represented in Fig. 3.

- Thermal noise due to resistors R_f, and R_{f2}: $v_{n,Rf}$ *and* $v_{n,Rf2}$.
- Thermal noise due to the channel admittance of M_{N1} and M_{P1}: $i_{n,MN1}$ and $i_{n,MP1}$.

The remaining noise sources were neglected assuming that the gain of the first stage is adequate. The equivalent noise voltage referred to the LNA input is given by,

$$\begin{cases} v_{n,Rs} = \dfrac{v_{n,Rf}}{R_f} Rs + \dfrac{i_{n,MN1} + i_{n,MP1}}{g_{m1}} + \dfrac{1}{g_{m1}} \dfrac{v_{n,Rf2}}{R_{f2}} \\ g_{m1} = g_{mN1} + g_{mP1} \end{cases} . \quad (4)$$

Using (4), the NF of the balun-LNA can be approximated by

$$\mathrm{NF} = 1 + \frac{v_{n,in}}{v_{n,Rs}} \approx 1 + \frac{R_S}{R_f} + \frac{1}{g_{m1} R_S} + \frac{1}{g_{m1}^2 R_{f2} R_S} . \quad (5)$$

From (5), we note that to improve the NF, the feedback resistor R_f and the transconductance of the first stage must be maximized. The optimized device sizes are listed in Table I.

TABLE I.
BALUN-LNA DEVICE SIZES.

Parameter	Value	Parameter	Value
M_{P1} (W/L)	600µm/0.18µm	R_F	450 Ω
M_{N1} (W/L)	300µm/0.18µm	R_{F2}	300 Ω
M_{P2} (W/L)	200µm/0.06µm	R_{F3}	225 Ω
M_{N2} (W/L)	100µm/0.06µm	$R_{d\{P,N\}3}$	70 Ω
M_{P3} (W/L)	400µm/0.06µm	$C_{d\{P,N\}3}$	500 fF
M_{N3} (W/L)	200µm/0.06µm		
$g_{m\{P,N\}1} \approx 22.0$ mS, $g_{m\{P,N\}2} \approx 12.5$ mS, $g_{m\{P,N\}3} \approx 14.5$ mS			
$I_D(M_{\{P,N\}1}) \approx 3.5$mA, $I_D(M_{\{P,N\}2}) \approx 1.8$mA, $I_D(M_{\{P,N\}1}) \approx 1.3$mA,			

TABLE II.
EFFECT OF THE FIRST STAGE TRANSISTOR LENGTH ON THE LNA PERFORMANCE.

	1st stage transistor length [nm]		
Parameter	60	120	180
Flat Gain [dB]	20.6	21.2	21.9
Spot NF@10 MHz [dB]	5.3	4.3	4.1
Spot NF@50 MHz [dB]	2.8	2.5	2.7
Spot NF@6 GHz [dB]	2.2	2.6	3.2
S11 bandwidth [GHz]	8.7	7.9	6.3
Power [mW]	10.1	8.4	7.9

IV. DESIGN VERIFICATION

The proposed circuit was designed and optimized in a 65-nm CMOS technology, and using a 1.2-V supply voltage. In table I, the sizing of the circuit is presented. The first stage has the largest transistor size, and consequently the highest transconductance and draws the largest amount of current. Besides, the transistors of the first stage should not be of minimum length to improve the NF at low frequencies (flicker noise is higher if minimum length transistors are used), and to reduce the power consumption. In table II, we list several LNA parameters, and show that depending on the specifications, the transistor's channel length of the first stage can be used to trade NF with bandwidth.

The voltage gain, NF and input impedance matching conditions are plotted in Fig. 4. The gain is approximately constant and equal to 21.2 dB, from low frequencies till 6 GHz. From the results of the three parameters we can estimate a bandwidth of operation between 20 MHz and 6 GHz, where we have impedance matching, a gain of 21.2 dB and a noise figure less than 3.2 dB.

In Fig. 5, the IIP_2 and IIP_3 of the proposed LNA are presented and compared with results from [5] and [6]. The IIP_2 of this work is considerably higher than that from previous works. The IIP_3 is in the order of previous works, but is much more constant along frequency than the others.

In Figs. 6 and 7, the effect of the variation of the degeneration capacitors and resistors of the third stage is

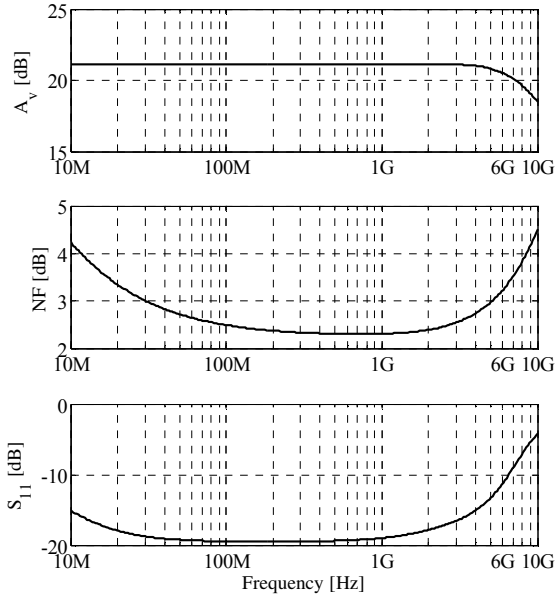

Fig. 4. Balun-LNA's voltage gain, A_v, noise figure, NF, and input impedance matching S_{11}.

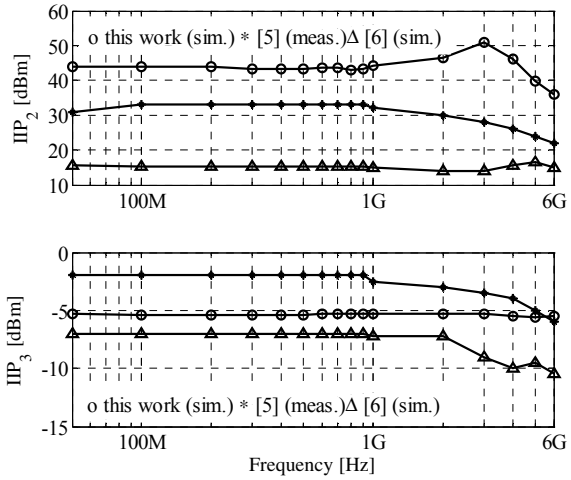

Fig. 5. IIP2 and IIP3 of the proposed balun-LNA, and comparison with results from [5] and [6].

presented. It is possible to see that the degeneration capacitors have a large effect on the output phase imbalance at high frequencies, while the degeneration resistors have a significant effect on the gain imbalance, especially at low frequencies.

With the values used in table I, i.e., $R_{d\{P,N\}3} = 70$ Ω, and $C_{d\{P,N\}3} = 500$ fF, the output gain and phase imbalances at 6 GHz are 2.6 dB and 3.8º, respectively.

The circuit presented in Fig. 8 can be used as the secondary LNA which takes advantage of capacitive cross-coupling as the differential gain-phase balancer [7]. With that circuit, the output gain and phase imbalance at 6 GHz are improved to 1.1 dB and 2.6º, respectively, at the expense of 2-mW extra power.

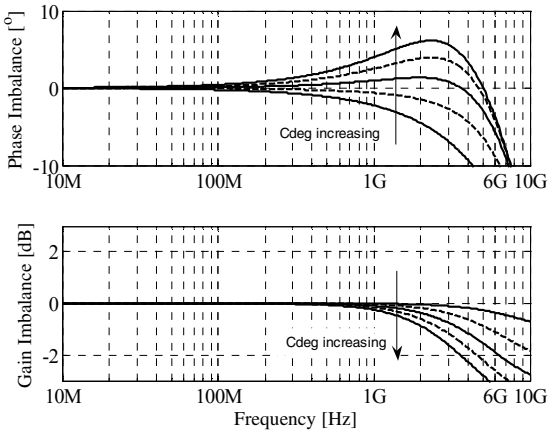

Fig. 6. Output gain and phase imbalance when the degeneration capacitors of the 3rd stage vary between 200 fF and 600 fF, with steps of 100 fF.

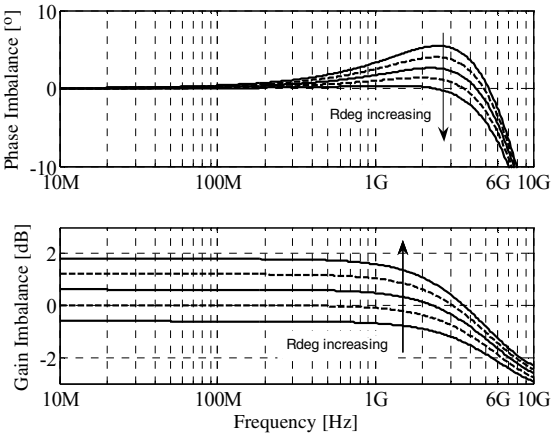

Fig. 7. Output gain and phase imbalance when the degeneration resistors vary between 60 Ω and 80 Ω, with steps of 5 Ω.

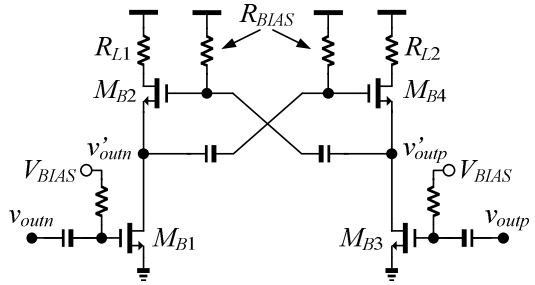

Fig.8. A secondary LNA can be utilized to further improve the balun-LNA's output gain-phase balancing.

Table III summarizes the main LNA performance metrics and compares them to the recently published works. We see that two main improvements of this new balun-LNA are the IIP_2 and the power consumption which are clearly enhanced.

V. Conclusions

An SDR balun-LNA employing cascade of inverter-based amplifiers with resistive feedback, pseudo-differential sensing and partial *RC* degeneration has been proposed. No inductor, explicit bias circuit or ac-coupling networks are entailed. Extensive simulations verified the feasibility of the circuit with respect to prior works. Throughout the covered band the simulated peak voltage gain is 21.2 dB whereas the noise figure is <3.2 dB. The IIP2 varies between 36.0 and 51.1 dBm and the IIP3 is around -5.4 dBm. The power consumption is 7.9 mW at 1.2 V.

TABLE III.
PERFORMANCE COMPARISON

	[5] *	[6]	This work
CMOS Tech.	65 nm	65 nm	65 nm
Bandwidth (GHz)	0.05-10	0.05-10	0.02-6
S_{11} (dB)	<-10	<-10	<-11
S_{21} (dB)	18-20	24-25	21.2
NF (dB)	2.9-5.9	2.7-3.6	<3.2
IIP_2 (dBm) (min/max)	14/ 19.5	10.2/32.4	36.0/51.1
IIP_3 (dBm) (min/max)	-11.2/-7	-10/-2	-5.6/-5.3
Power (mW)	22	21.7	7.9

* Measurement results

Acknowledgement

The authors would like to acknowledge the following institutions: TES Electronic Solutions, INESC-ID and University of Macau. This work was supported by the Research Committee of the University of Macau, Macao Science and Technology Development Fund (FDCT), and by the Portuguese Foundation for Science and Technology (FCT)) through PIDDAC Program Funds and SCOMagNo (PTDC/CTM-NAN/112672/2009).

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