Analysis and Design of Open-Loop Multiphase Local-Oscillator Generator for Wireless Applications

Ka-Fai Un, *Student Member, IEEE*, Pui-In Mak, *Member, IEEE*, and Rui P. Martins, *Fellow, IEEE*

***Abstract*—Multiphase local-oscillator (LO) generators have been widely adopted in modern wireless communication systems. This paper describes the analysis and design of two open-loop multiphase (quadri and octave) LO generators, which can lead to speed relaxation of the phase-locked loop and voltage-controlled oscillator when compared with conventional frequency-division methods. The mathematical model, sizing considerations, and two design examples targeting mobile-TV applications are presented. The first one is an octave-phase LO generator designed in 90-nm CMOS featuring multiple switchable phase correctors in cascade. It covers the VHF-III and UHF bands with an optimized phase precision within 0.8°. The second one combines quadri- and octave-phase LO generation to cover the full band of mobile TV from 170 to 1700 MHz. Optimized in 65-nm CMOS, it can be operated in octave-phase mode for image-reject harmonic-reject downconversion or in quadri-phase mode for simple image-reject downconversion. Extensive simulations accounting for process variations show that the achieved phase precisions are within 1.5° (quadri) and 1° (octave). The phase-noise performance is comparable with state-of-the-art solutions.**

***Index Terms*—CMOS, harmonic-reject mixer, image-reject mixer, mobile-TV tuner, multiphase local-oscillator (LO) generator, phase-locked loop (PLL), radio frequency (RF), voltage-controlled oscillator (VCO)**

I. Introduction

MODERN wireless communication systems are urged to become multistandard compliant, low cost, and low power. Hardware reuse and compact realization resorting from advanced nanoscale processes are the key trends to reach those goals. For mobile-TV applications [1], [2], the most dominant standards are DVB-H, T-DMB, ISDB-T, and MediaFLO. They are spread over the VHF-III band (170–245 MHz), UHF band (470–860 MHz), and L-band (1400–1700 MHz). A direct-conversion topology [3] with wideband radio-frequency (RF) circuits [4] appears as an optimum way to realize multistandard compliant systems at low cost. One key design challenge lies on RF downconversion. Hard-switching mixers suffer from the problem of harmonic mixing [5] in the VHF-III and UHF bands, as shown in Fig. 1(a). With no prefiltering, the in-band blockers located at the odd harmonics of the local oscillator (LO), particularly the strong third and fifth harmonics, become the cochannel interferers after downconversion. To overcome such a hindrance, a harmonic-reject mixer [6], [7] was introduced with the intent of interpolating a pseudo LO with no third and fifth harmonics. Together with the requirement of image rejection, the downconversion scheme will include two channels: in-phase (I) and quadrature (Q), as shown in Fig. 1(b). Each channel is synthesized by three parallel paths having a gain ratio of $1:\sqrt{2}:1$. An octave-phase LO is required for the VHF-III and UHF bands to support image-reject harmonic-reject downconversion. On the other hand, since the harmonics of the L-band are located at sufficiently high frequency, only image-reject downconversion is entailed. In this case, such a downconversion scheme can be simplified to work with a quadri-phase LO, i.e., only P0° and P90° are needed for the I and Q channels, respectively.

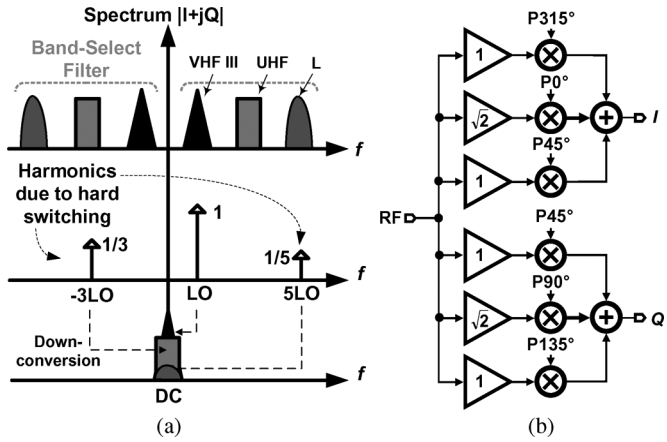

Fig. 1. (a) Harmonic mixing in a wideband mobile-TV receiver. (b) Image-reject harmonic-reject downconversion scheme.

Many different types of multiphase LO/clock generators have been proposed for wireless and wireline applications. A ring voltage-controlled oscillator (VCO) using inverters [Fig. 2(a)] is a compact solution to realize a multiphase LO with a large frequency range [8], [9]. However, its phase-noise performance is normally unacceptable for high-tier wireless systems. Although the phase noise can be substantially reduced by replacing all inverters with LC VCOs [Fig. 2(b)], the associated inductors occupy lots of chip area [10], [11]. Delay-locked loop (DLL) using numerous delay units can also be a multiphase clock generator [Fig. 2(c)] [12], [13]. The key drawback is that the phase-

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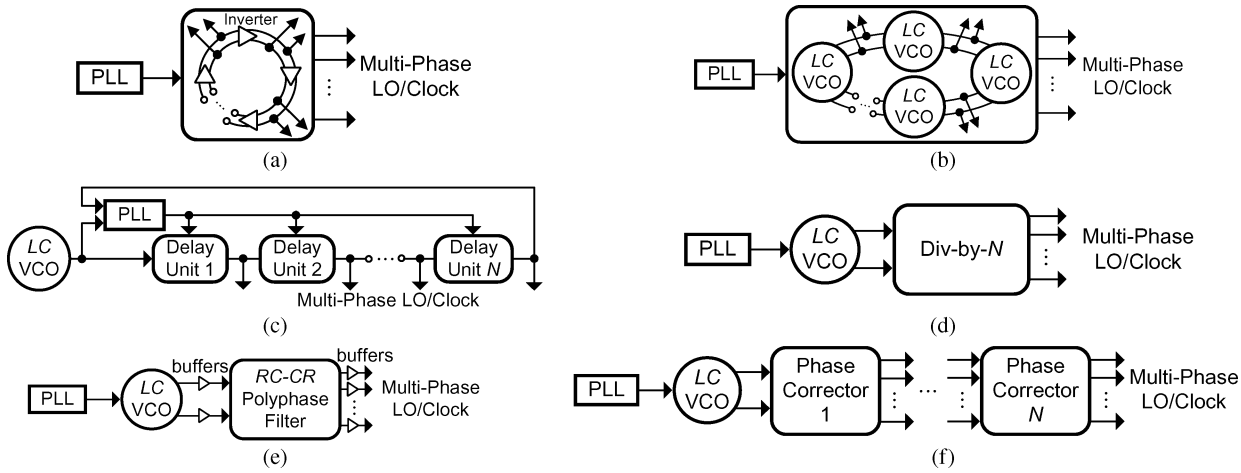

Fig. 2. Multiphase LO/clock generation methods. (a) Ring with inverters. (b) Ring with LC VCOs. (c) DLL. (d) Frequency divider. (e) $RC-CR$ polyphase filter. (f) Phase correctors in cascade.

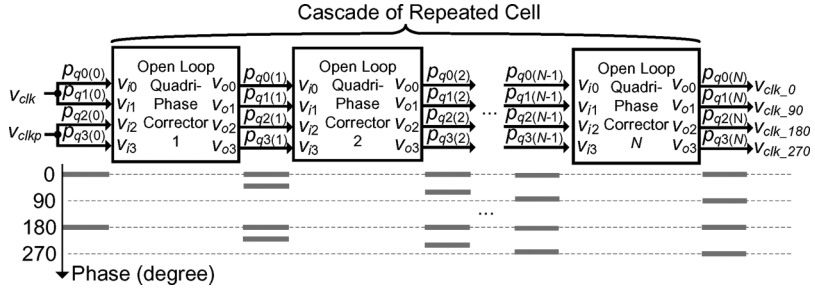

Fig. 3. Block diagram of a quadri-phase LO generator. Phase error is reduced progressively from correctors 1 to N.

noise performance is heavily dependent on the number of output phases required.

Alternatively, a multiphase LO signal can be generated in an open-loop way by using a low-noise LC VCO, followed by a frequency divider [Fig. 2(d)] [12]. Elementarily, a quadri-phase LO can be generated by using a divide-by-two circuit. Such a division factor implies that the associated phase-locked loop (PLL) and VCO have to operate at a doubled frequency. The design complexity, however, rises dramatically with the number of phases required. For instance, to generate an octave-phase LO, a divide-by-four circuit is necessary, while the PLL and VCO have to operate at four times of the output frequency. A higher operating frequency unavoidably calls for more power to lower the phase noise and phase error. Moreover, the PLL and VCO will be more sensitive to parasitic capacitances, implying narrower locking and tuning ranges, respectively. To surmount these constraints, the frequency divider can be replaced by a passive $RC-CR$ polyphase filter [Fig. 2(e)] [14], [15], but the performance can be strongly affected by temperature and process variations, while power-hungry buffers are required for a proper interface. Recently, an open-loop quadri-phase clock generator was proposed for wireline applications [16], [17]. Multiple phase correctors are cascaded in an open-loop way to improve the phase precision [Fig. 2(f)]. The prime advantages of this method are its simplicity (i.e., open loop and inverter only), no power-hungry buffer, the independence of the number of output phases to the operation frequency of the circuit itself, and its driving source. The achieved frequency range in [16] is 0.37–2.5 GHz, and the phase precision is $\pm 5^\circ$ for a quadri-phase output.

This paper extends the concept of such an open-loop architecture for wireless applications with different requirements on the phase precision and the number of output phases [18]. The targeted phase error is $\pm 1^\circ$, and both quadri- and octave-phase LO generators will be designed and analyzed. The mathematical model, design considerations, and the respective implementation constitute the originality of this paper.

Section II presents the mathematical model and design considerations of the open-loop quadri- and octave-phase LO generators. Two design examples with extensive simulation results for validating the feasibility of the proposed techniques are addressed in Section III. Section IV concludes this paper.

II. Mathematical Model and Design Considerations of the Open-Loop Quadri- and Octave-Phase LO Generators

A. Quadri-Phase LO Generator

Architecture: The block diagram of a quadri-phase LO generator is shown in Fig. 3. It is structured by putting numerous phase correctors in cascade to interpolate a multiphase LO from a two-phase differential input ($v_{\rm clk}$ and $v_{\rm clkp}$). From left to right, the phase correctors improve the phase precision progressively until reaching the desired accuracy. The schematic of each inverter-based quadri-phase corrector is shown in Fig. 4. Every corrector is composed of 16 inverters (CMOS) classified according to two different device sizes as L or S type. L-type inverters feature a larger geometrical size than the S-type ones to optimize the phase precision in a specific frequency range. The inverters can be divided into three groups according to their

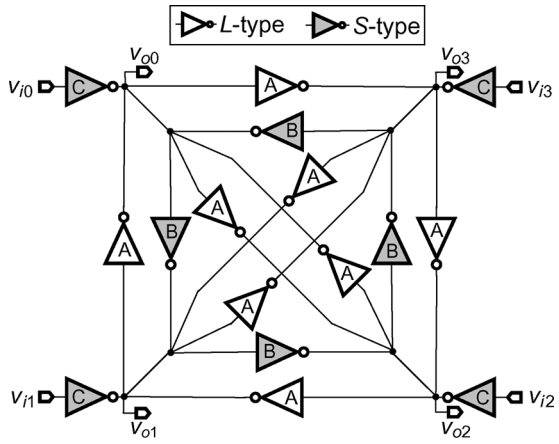

Fig. 4. Architecture schematic of an inverter-based quadri-phase corrector.

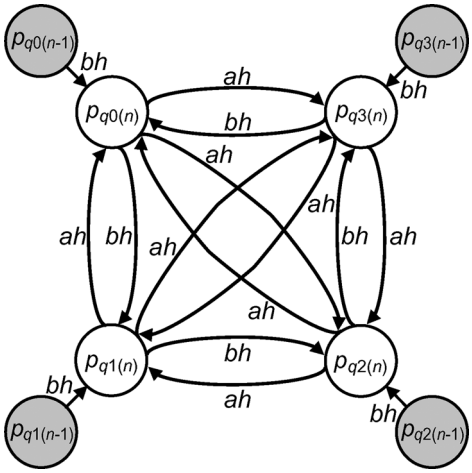

Fig. 5. SFG of a quadri-phase corrector.

functionality: 1) Set **A** is for phase correction. With three inverters in a loop, it is able to oscillate and interpolate the intermediate phases; 2) set **B** is for natural-frequency suppression; it leads to a larger operating frequency range [16]; 3) set **C** is for signal injection; it allows multiple phase correctors to be directly cascaded to improve the output-phase precision.

Mathematical Model: In order to determine the optimum conditions in terms of frequency range and phase precision, the quadri-phase corrector is modeled by a signal flow graph (SFG), as shown in Fig. 5. For simplicity, a linear model is assumed [19], [20]. Each inverter is modeled as a single-pole amplifier with a transfer function of $h(f)$, as given by

$$h(f) = -\frac{G}{1 + \frac{jf}{f_C}} \tag{1}$$

where G is the normalized dc gain and f_C is the -3-dB cutoff frequency. The constants a and b in Fig. 5 represent the driving capabilities of L- and S-type inverters, respectively [18].

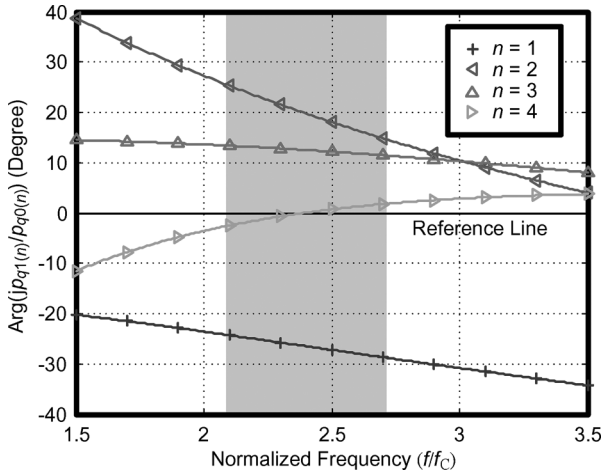

Fig. 6. Static phase error of a quadri-phase corrector with $a/b = 3.4$ and $G = 10$ (linear-model simulation).

Phasor-domain analysis is applied to obtain the phase correction transformation of the nth phase corrector, as expressed by

$$\begin{cases} A_q p_{q(n)} = p_{q(n-1)} \\ A_q = \begin{bmatrix} 1 & -ah & -ah & -bh \\ -bh & 1 & -ah & -ah \\ -ah & -bh & 1 & -ah \\ -ah & -ah & -bh & 1 \end{bmatrix} \\ p_{q(n)} = \begin{bmatrix} p_{q0(n)} & p_{q1(n)} & p_{q2(n)} & p_{q3(n)} \end{bmatrix}^{\mathrm{T}} \end{cases} \tag{2}$$

where A_q is the phase transformation matrix and $p_q(n)$ is the output-phase vector. Rearranging (2) yields

$$p_{q(n)} = A_q^{-1} p_{q(n-1)}. \tag{3}$$

For N quadri-phase cascaded correctors, $p_{q(N)}$ becomes

$$p_{q(N)} = A_q^{-N} p_{q(0)} \tag{4}$$

where $p_{\mathrm{q(0)}}$ is the input-phase vector represented by

$$p_{q(0)} = \begin{bmatrix} 1 & 1 & -1 & -1 \end{bmatrix}^{\mathrm{T}} bh \tag{5}$$

since the input phase can be either 0° or 180°. In the phasor domain, only 1 or -1 is available for the input vector. Fig. 6 shows the steady-state phase-error function defined by (6) with different number of stages in cascade

$$\Phi_{eq(n)} = Arg\left(j\frac{p_{q1(n)}}{p_{q0(n)}}\right) \tag{6}$$

where a/b is chosen to be 3.4 to provide an acceptable frequency range and G is selected as ten (practical dc gain value of a CMOS inverter in nanometer technologies). The steady-state phase error depends on the ratio of the output frequency (f) to the corner frequency of an inverter (f_c), as well as the number (n) of phase correctors in cascade. With $n = 4$, the phase error is minimized over a wide range of f/f_c (between 2.1 and 2.7).

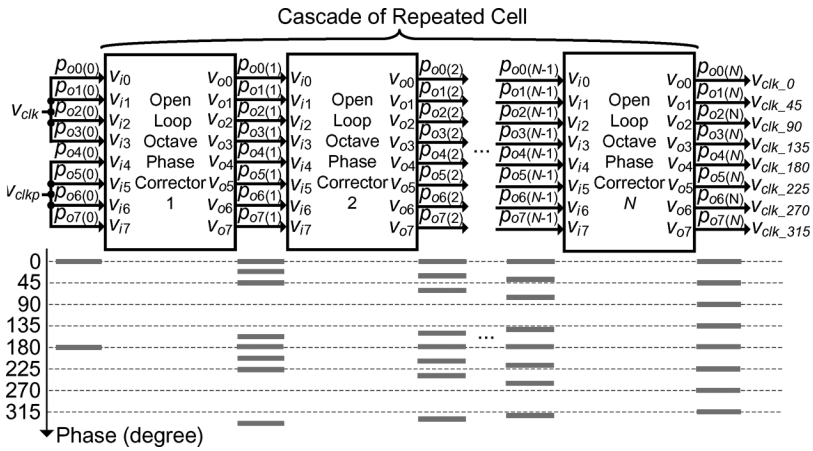

Fig. 7. Block diagram of an octave-phase LO generator.

Fig. 6 also shows that the steady-state phase error can be minimized by cascading additional stages of quadri-phase correctors for certain frequency ranges.

Based on the aforementioned definitions and following a particular context, the transfer function of the linearized quadri-phase LO generator will be derived next. According to it, the optimal conditions for minimizing the phase error are obtained to build up the device-sizing strategy.

From (2), we can simply prove that

$$\begin{cases} p_{q0(n)} = -p_{q2(n)} \\ p_{q1(n)} = -p_{q3(n)}. \end{cases} \tag{7}$$

Thus, (2) and (3) can be simplified as

$$\begin{bmatrix} 1+ah & -(a-b)h \\ (a-b)h & 1+ah \end{bmatrix} \begin{bmatrix} p_{q0(n)} \\ p_{q1(n)} \end{bmatrix} = \begin{bmatrix} p_{q0(n-1)} \\ p_{q1(n-1)} \end{bmatrix}. \tag{8}$$

In addition, for a simplification of the notations, A, B, and C are introduced as follows:

$$\begin{aligned} A &= 1+ah \\ B &= (a-b)h \\ C &= \begin{bmatrix} A & -B \\ B & A \end{bmatrix}. \end{aligned} \tag{9}$$

Similar to (4), we can obtain

$$\begin{bmatrix} p_{q0(N)} \\ p_{q1(N)} \end{bmatrix} = C^{-N} \begin{bmatrix} p_{q0(0)} \\ p_{q1(0)} \end{bmatrix} = C^{-N} \begin{bmatrix} 1 \\ 1 \end{bmatrix}. \tag{10}$$

Since the matrix C can be diagonalized as

$$C = \left(\frac{1}{\sqrt{2}} \begin{bmatrix} j & -j \\ 1 & 1 \end{bmatrix} \right) \begin{bmatrix} A+jB & 0 \\ 0 & A-jB \end{bmatrix} \left(\frac{1}{\sqrt{2}} \begin{bmatrix} -j & 1 \\ j & 1 \end{bmatrix} \right) \tag{11}$$

substituting it into (10) will finally lead to

$$\begin{bmatrix} p_{q0(N)} \\ p_{q1(N)} \end{bmatrix} = 2^N \begin{bmatrix} (1+j)(A+jB)^{-N} + (1-j)(A-jB)^{-N} \\ (1-j)(A+jB)^{-N} + (1+j)(A-jB)^{-N} \end{bmatrix}. \tag{12}$$

Finally, the transfer function of $p_{q1(N)}$ divided by $p_{q0(N)}$ can be obtained as

$$\frac{p_{q1(N)}}{p_{q0(N)}} = \frac{j + \left(\frac{1+ah-j(a-b)h}{1+ah+j(a-b)h} \right)^N}{1 + j \left(\frac{1+ah-j(a-b)h}{1+ah+j(a-b)h} \right)^N}. \tag{13}$$

The criterion for phase-error minimization is equivalent to setting

$$\frac{p_{q1(1)}}{p_{q0(1)}} = -j \tag{14}$$

which implies a 90° phase shift. Substituting (14) into (13) leads to

$$\begin{cases} 1 - 2Ga + Gb + \frac{f}{f_c} = 0 \\ 1 - Gb - \frac{f}{f_c} = 0. \end{cases} \tag{15}$$

By solving (15), the optimal conditions for phase-error minimization can be obtained as

$$\begin{cases} a = G^{-1} \\ f = G(a-b) f_c. \end{cases} \tag{16}$$

It implies that an ideal 90° phase shift happens at the natural frequency of the circuit: $f_n = G(a-b)f_c$. Also, a larger a/b ratio can provide a stronger phase-correcting ability.

B. Octave-Phase LO Generator

Architecture: Octave-phase LO generation can be obtained by further extending the quadri-phase LO concept and architecture previously outlined. As such, the block diagram of an octave-phase LO generator can be drawn, as shown by Fig. 7. From left to right, an octave-phase LO can be composed of multiple octave-phase correctors. The number of stages in cascade will directly depend on the final phase-precision requirement. The architecture schematic of an octave-phase corrector is shown in Fig. 8, which is composed of 32 inverters (CMOS). Similar to the quadri-phase design, the inverters are also classified as either L or S type, and the three sets ($\mathbf{A}$, $\mathbf{B}$, and $\mathbf{C}$) previously mentioned are also maintained.

Mathematical Model: The SFG of the octave-phase corrector is shown in Fig. 9, where a linear model is also assumed and

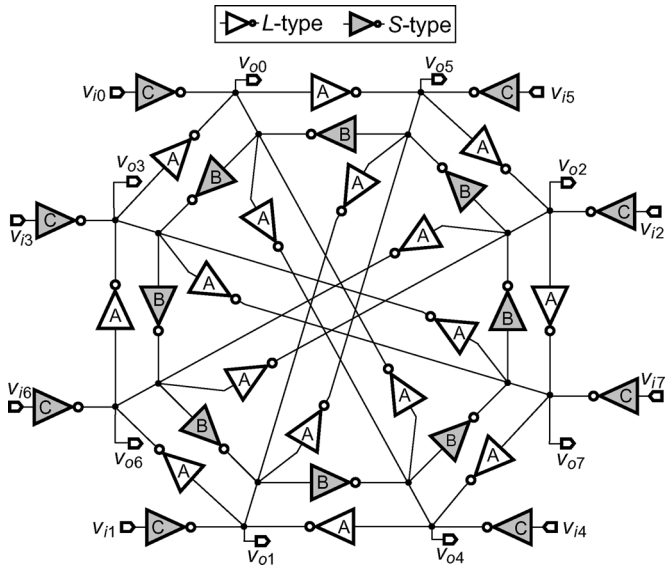

Fig. 8. Architecture schematic of an octave-phase corrector.

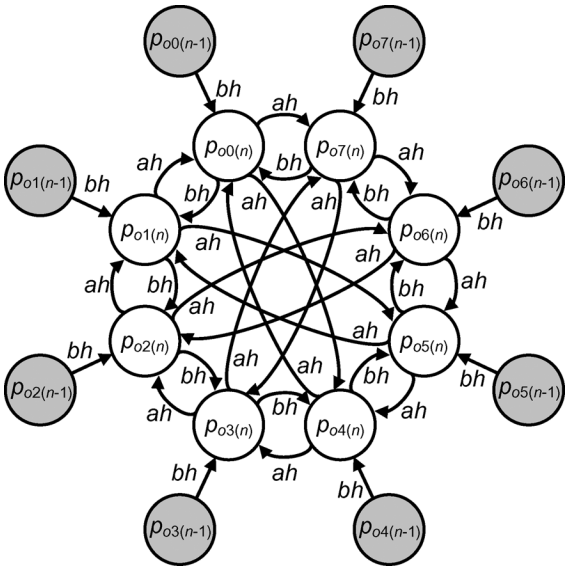

Fig. 9. SFG of an octave-phase corrector.

each inverter is modeled similarly as a single-pole amplifier. Again, phasor-domain analysis is applied to obtain the phase transformation of the nth octave-phase corrector, as given by

$$\begin{cases} A_o p_{o(n)} = p_{o(n-1)} \\ A_o = \begin{bmatrix} 1 & -ah & 0 & 0 & -ah & 0 & 0 & -bh \\ -bh & 1 & -ah & 0 & 0 & -ah & 0 & 0 \\ 0 & -bh & 1 & -ah & 0 & 0 & -ah & 0 \\ 0 & 0 & -bh & 1 & -ah & 0 & 0 & -ah \\ -ah & 0 & 0 & -bh & 1 & -ah & 0 & 0 \\ 0 & -ah & 0 & 0 & -bh & 1 & -ah & 0 \\ 0 & 0 & -ah & 0 & 0 & -bh & 1 & -ah \\ -ah & 0 & 0 & -ah & 0 & 0 & -bh & 1 \end{bmatrix} \\ p_{o(n)} = [p_{o0(n)} \quad p_{o1(n)} \quad \cdots \quad p_{o7(n)}]^{\mathrm{T}} \end{cases} \tag{17}$$

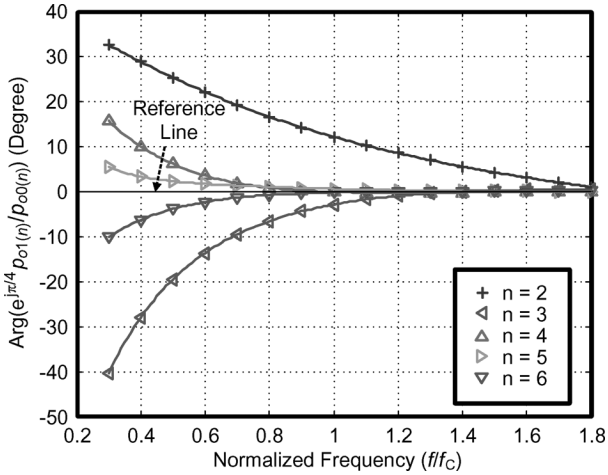

Fig. 10. Static phase error of an octave-phase corrector with $a/b = 3.5$ and $G = 10$ (linear-model simulation).

where A_o is the octave-phase transformation matrix and $p_{o(n)}$ is the output-phase vector of the nth octave-phase corrector. Rearranging (17) will yield

$$p_{o(n)} = A_o^{-1} p_{o(n-1)}. \tag{18}$$

For N octave-phase correctors in cascade, $p_{o(N)}$ is given by

$$p_{o(N)} = A_o^{-N} p_{o(0)} \tag{19}$$

where $p_{o(0)}$ is the input-phase vector

$$p_{o(0)} = [1 \quad 1 \quad 1 \quad 1 \quad -1 \quad -1 \quad -1 \quad -1]^{\mathrm{T}} bh \tag{20}$$

since the input phase can be either 0° or 180°. In the phasor domain, only 1 or -1 is available for the input-phase vector. The steady-state phase-error function can be defined by

$$\Phi_{eo(n)} = Arg\left(e^{\frac{j\pi}{4}} \frac{p_{o1(n)}}{p_{o0(n)}}\right). \tag{21}$$

As shown by Fig. 10, the steady-state phase error can be minimized by cascading additional stages of octave-phase correctors for a certain frequency range from 0.7 to 1.3 (normalized frequency: f/f_c). The a/b ratio is set to be 3.5, and G is ten. Although the optimum conditions in terms of frequency range and phase precision can be derived from the linear model, the final phase permutation can only be determined from transistor-level simulation because not all transistors can be operated simultaneously in the saturation region (further analysis of this issue is presented in the Appendix).

C. Design Considerations

Sizing: Both quadri- and octave-phase correctors have a limited operating frequency range. The channel length of the inverter's transistors is correlated to the upper frequency limit (i.e., a smaller channel length allows a higher operating frequency). When the channel length is fixed, the a/b ratio is correlated to the range and the phase-correcting ability of the phase corrector. A smaller a/b ratio can increase its operating range

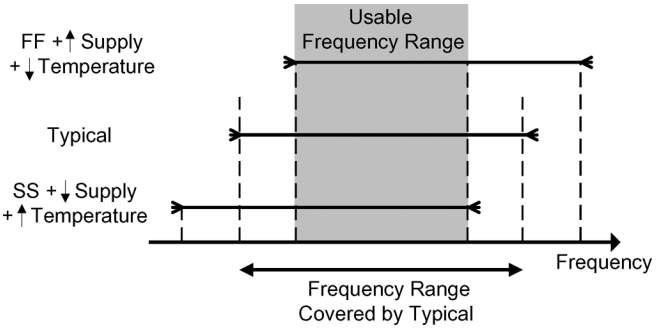

Fig. 11. Usable frequency range accounting for PVT variations.

at the expense of a weaker phase-correcting ability. Thus, subject to different applications, the optimum a/b ratio should be chosen such that the desired frequency range can be covered. On the other hand, the optimum number of phase correctors needed in cascade can be determined according to the required phase precision.

PVT Variations: Similar to the ring oscillator, the frequency range covered by the phase corrector can be sensitive to process, voltage, and temperature (PVT) variations. For fast–fast (FF)/slow-slow (SS) process corner with temperature and voltage variations, the covered frequency range is shifted up/down significantly, as shown in Fig. 11. For a reliable design, the channel length of the inverters is determined at "SS corner + low supply voltage + high temperature" for the highest operating frequency to be larger than the desired frequency. Then, a suitable a/b at "FF corner + high supply voltage + low temperature" is chosen for the lowest operating frequency, which is also lower than the desired. Increasing the width of the transistors can only lead to a better variability control at the expense of power. The operating principle is not dependent on the transistors' width.

Again, similar to the ring oscillator, the robustness of the phase corrector can be improved by adopting a supply regulator and a bandgap reference to cope with voltage and temperature variations, respectively [21], [22]. Simulations show that the regulator should stabilize the power supply with less than 80-mV fluctuation such that the phase noise of the multiphased LO will not be degraded by more than 1 dB at 1-MHz frequency offset. Those schemes are under development and have not been included in this paper.

Design and Verification Flow: The design and verification flow is graphically shown in Fig. 12(a) and (b). For simplicity, only the quadri-phase LO generator is considered. Based on the developed linear model and equations, the phase-error vector can be determined with initial values of G, a/b ratio, and n. These values can be adjusted to minimize the phase error over the desired frequency range with fast simulation speed. The obtained circuit parameters are then transferred to the transistor-level design. Since the circuit is dynamic, the optimization involves mostly transient simulations, except for the particular case of the phase noise that was checked through periodic noise (pnoise) simulations. Although the linear model can provide a set of parameters that are close to the optimum values, transistor-level fine-tuning is still necessary to account for PVT variations. Circuit nonlinearity may also affect the final phase permutation, and it must be confirmed at the transistor level. Finally, the optimized circuit can be transferred to the layout

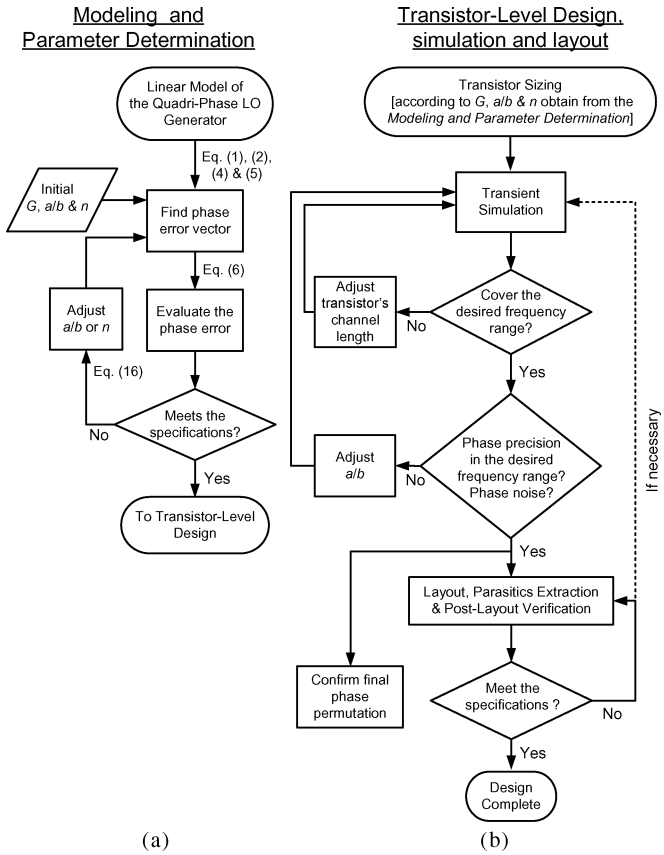

Fig. 12. Design and verification flow. (a) Modeling and parameter determination. (b) Transistor-level design, simulation, and layout.

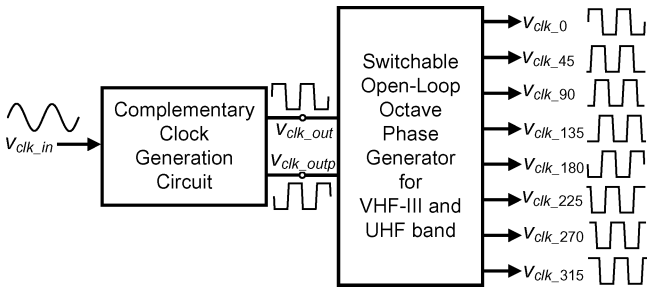

Fig. 13. Block schematic of design example 1 (octave-phase LO generator).

design phase. Postlayout verification with parasitic effects is needed to reconfirm all performance metrics, and it will be repeated until all specifications are met.

III. Design Examples and Simulation Results

A. Design Example 1—An Octave-Phase LO Generator for VHF-III and UHF Bands of Mobile TV in 90-nm CMOS

Circuit Schematics: An octave-phase LO is required for image-reject harmonic-reject downconversion in the VHF-III and UHF bands. High-precision-matched correlated phases are critical to achieve a high image-rejection ratio and a high harmonic-rejection ratio. The block diagram of design example 1 is shown in Fig. 13. The complementary clock generation circuit [23], [24] shown in Fig. 14(a) is used as the input stage, and the required input signal is a single-phase sinewave [25]–[27]. The optimum $R_{1,2}$ and $C_{1,2}$ values accounting for process variations are 10.5 kΩ and 1 pF, respectively. The

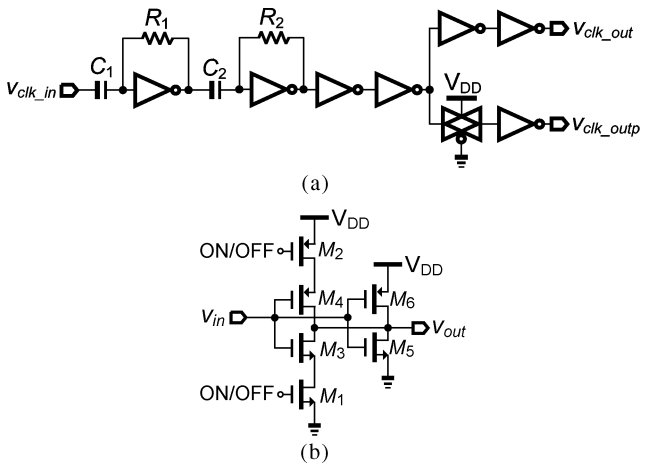

Fig. 14. Circuit schematics of (a) the complementary clock generator and (b) the dual-mode inverter employed into the octave-phase corrector.

TABLE I
SIZES OF THE TRANSISTORS IN FIG. 14(B)

Symbol	W/L (μm)	
	L-type inverter	*S*-type inverter
M_1	0.42/0.1	0.14/0.1
M_2	1.26/0.1	0.42/0.1
M_3	0.42/0.1	0.14/0.1
M_4	1.26/0.1	0.42/0.1
M_5	0.42/0.28	0.14/0.28
M_6	1.26/0.28	0.42/0.28

octave-phase LO generator has a limited frequency locking range. In order to extend it with minimal power consumption, the inverters within the phase correctors are designed to provide dual modes, as shown in Fig. 14(b). The transistors M_1 and M_2 are used as switches, where, if M_1 and M_2 are switched off, the phase generator works for the VHF-III band. If they are switched on, the phase generator works for the UHF band. The sizes of the dual-mode inverter transistors are listed in Table I. In this design, seven phase correctors are cascaded to meet the targeted phase precision.

Simulation Results: The phase-error functions are defined by the phase differences between $v_{\mathrm{clk\_0}}$ and $v_{\mathrm{clk\_45}}$ $(v_{\mathrm{clk\_90}}, v_{\mathrm{clk\_135}}, \ldots, v_{\mathrm{clk\_315}})$ subtracting the ideal phase differences. Fig. 15 shows the power dissipation versus the operating frequency in the VHF-III and UHF bands. Typically, the dynamic power consumption ranges from 2.3 to 5.1 mW, excluding that consumed by the output driving buffers. The phase-error simulation results over the desired operating frequencies and different process corners show that the phase precision is optimized to be within $\pm 0.8^{\circ}$ for process corners typical–typical (TT), FF, SS, fast-slow (FS), and slow-fast (SF) at room temperature and standard supply voltage. The performance summary of the overall octave-phase LO is given in Table II.

B. Design Example 2—A Quadri-/Octave-Phase LO Generator for Full-Band Mobile TV in 65-nm CMOS

Circuit Schematics: Covering the full band of mobile TV requires both quadri- and octave-phase LOs since L-band only requires image-reject downconversion. The multiphase LO generator combining quadri- and octave-phase techniques is shown in Fig. 16. The switchable topology, as shown in Fig. 14(b), is not applied here to minimize the parasitic capacitances in each path. Moreover, with three independent paths, the frequency range and precision can be optimized. Since a *differential* harmonic-reject mixer requires 12 LO-signal pins, a MUX with a dedicated circuit logic arrangement is used to obtain the clock

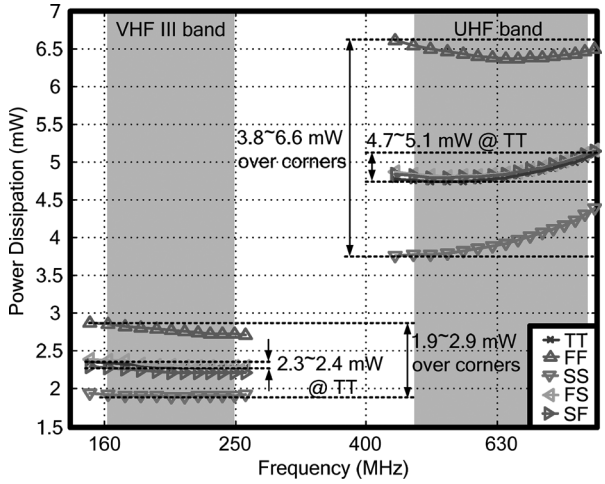

Fig. 15. Dynamic power dissipation of the octave-phase generator against process variations (schematic simulation).

TABLE II
PERFORMANCE SUMMARY OF DESIGN EXAMPLE 1 (SCHEMATIC SIMULATION)

Technology	90-nm CMOS
Supply Voltage	1 V
Power Dissipation (excluding O/P buffer)	2.3 – 5.1 mW
Operating Frequency Range	170 – 245 MHz (VHF-III band) 470 – 860 MHz (UHF band)
Number of Phases	Octave-phase
Maximum Absolute Phase Error	0.8°

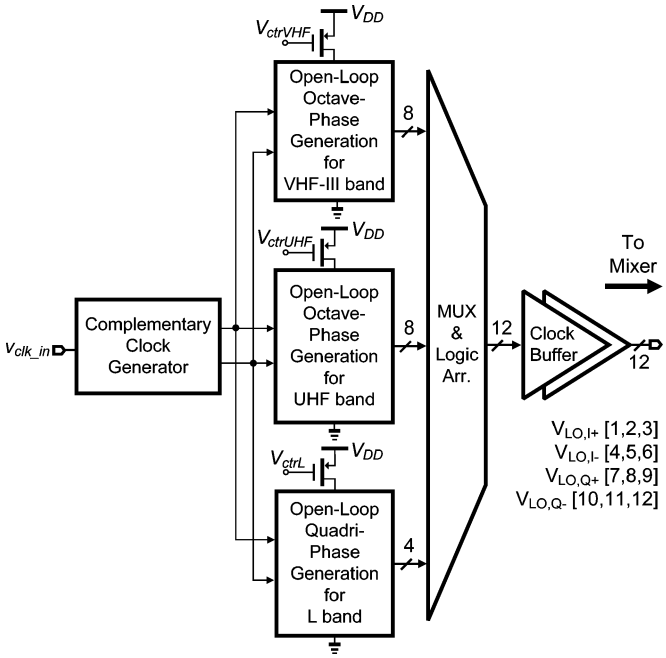

Fig. 16. Block schematic of design example 2 (quadri-/octave-phase generator).

TABLE III
PHASE ARRANGEMENT OF DESIGN EXAMPLE 2

Pin no.		VHF-III Band	UHF Band	L Band
$V_{LO,I+}$	1	0°	0°	0°
	2	45°	45°	0°
	3	90°	90°	0°
$V_{LO,I-}$	4	180°	180°	180°
	5	225°	225°	180°
	6	270°	270°	180°
$V_{LO,Q+}$	7	90°	90°	90°
	8	135°	135°	90°
	9	180°	180°	90°
$V_{LO,Q-}$	10	270°	270°	270°
	11	315°	315°	270°
	12	0°	0°	270°

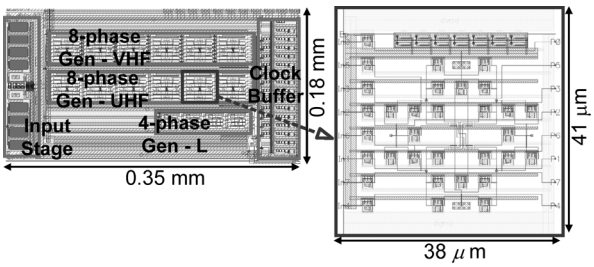

Fig. 17. Layout of the quadri-/octave-phase generation circuit.

TABLE IV
COMPONENT SIZES OF THE INVERTERS IN DESIGN EXAMPLE 2

Transistor		W/L (μm)	
		L-type inverter	*S*-type inverter
VHF-III Band	PMOS	1.080/0.33	0.270/0.33
	NMOS	0.540/0.33	0.135/0.33
UHF Band	PMOS	0.980/0.06	0.280/0.06
	NMOS	0.490/0.06	0.140/0.06
L Band	PMOS	0.920/0.06	0.270/0.06
	NMOS	0.460/0.06	0.135/0.06

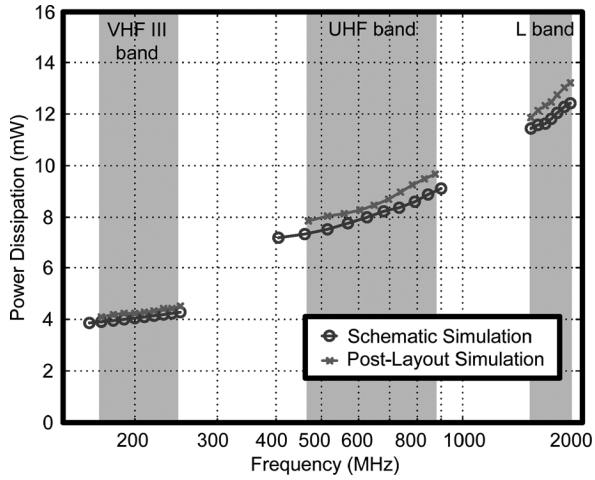

Fig. 18. Dynamic power dissipation of the quadri-/octave-phase LO generator with output buffers (schematic and postlayout simulations).

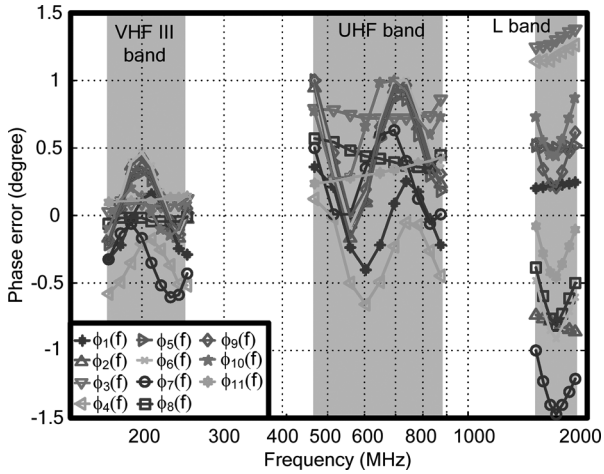

Fig. 19. Phase errors of the generated signals at TT corner (postlayout simulations).

signal according to Table III. In this case, the downconversion scheme is switchable between octave- and quadri-phase mixings. The layouts of the multiphase LO generator and one octave-phase corrector are shown in Fig. 17. The place and route of each phase corrector is optimized for minimization of the parasitic mismatch between different output nodes. The total active area is 0.063 mm^2. Each corrector occupies $< 0.0016\,\text{mm}^2$. The inverter transistors' sizes are listed in Table IV. The optimized numbers of stages for octave- and quadri-phase generation are six and four, respectively. This work is part of a full-band mobile-TV tuner that is currently under fabrication. Experimental results such as harmonic-reject ratio will further demonstrate the phase precision at the system level.

Simulation Results: The phase-error functions are defined by the phase differences between $v_{\text{clkout}[0]}$ and $v_{\text{clkout}[1]}$ $\left(v_{\text{clkout}[2]}, v_{\text{clkout}[3]}, \ldots, v_{\text{clkout}[11]}\right)$ subtracting the ideal phase differences. Fig. 18 shows the power dissipation versus the operating frequency in the VHF-III, UHF, and L-bands. Typically, the dynamic power consumption ranges from 4.1 to 13.2 mW (postlayout with parasitic-capacitance extraction), including that consumed by the output driving buffers. Since the output clock signals exhibit a fast rise/fall time (as fast as 20 ps), most of the power is consumed by the output buffer. The core phase correctors consume in total around 3 mW at TT corner, with $\pm 30\%$ among all corners.

The postlayout simulation results of the phase errors at TT corner are shown in Fig. 19. The octave-phase precisions are within 1° for the VHF-III and UHF bands. The quadri-phase precisions are within 1.5° for the L-band mode. These phase precisions fairly meet the design target, and the simulated results deviate from the calculated model with less than 0.5° over the desired frequency range. The phase-error degradation after layout is mainly derived from different parasitic capacitances associated with each interconnect node. Layout optimization with optimum placement of each inverter and conservative parasitic RC extraction can further minimize the systematic phase offset. Since the phase precision is determined by the transistor intrinsic RC value, which is sensitive to the parasitic capacitance, the circuit must be carefully laid out and extracted to tune out this effect by using the back-annotation function. The phase-error simulation results over the desired operating frequencies and different process corners show that the phase precision is optimized to be within $\pm 1°$ for all process corners. The performance summary of design example 2 is given in Table V.

Another issue inherent to wireless communication systems is the phase noise penalized by the multiphase LO generator. In

TABLE V
PERFORMANCE SUMMARY OF DESIGN EXAMPLE 2 (POSTLAYOUT SIMULATION)

Technology	65-nm CMOS
Supply Voltage	1.1 V
Power Dissipation	4.1 – 13.2 mW
Load Capacitance	50 fF
Operating Frequency Range	170 – 245 MHz (VHF-III band) 470 – 860 MHz (UHF band) 1.4 – 1.7 GHz (L band)
Number of Phases	Octave-phase for VHF-III and UHF bands, Quadri-phase for L band
Maximum Absolute Phase Error	1° for Octave-phase 1.5° for Quadri-phase

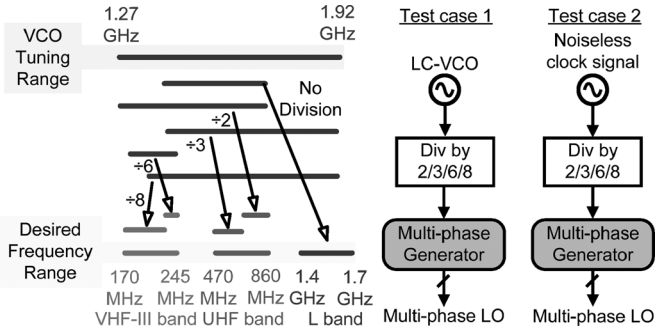

Fig. 20. Frequency plan of the entire multiphase LO generation scheme.

order to examine it, an inductor–capacitor voltage-control oscillator (LC-VCO) and reconfigurable frequency dividers have been designed for testability of design example 2. With the frequency plan shown in Fig. 20, the LC-VCO is optimized to cover a frequency range of 1.25–1.95 GHz using switched-capacitor banks and varactors. The L-band requires no division, whereas the VHF-III and UHF bands can be covered optimally with the most efficient frequency division ratios, as it does not link with the number of output phases. In this particular example, divide-by-/two/three/six/eight balances the tuning range and phase noise of the LC-VCO. Another test case is related with the replacement of the LC-VCO by a noiseless source so that we can clearly quantify the noise injected by the multiphase LO generator. The simulated phase noises of the VCO, sources after division, and at the output of the multiphase LO generator are shown in Fig. 21(a)–(c) for the VHF-III, UHF, and L-bands, respectively. The phase noise is mainly degraded at far-out frequency ranges being -137 dBc/Hz at 1-MHz offset for the VHF-III band. A similar observation holds for the UHF and L-bands since the phase noises at 1-MHz offset are -129.1 and -124.9 dBc/Hz, respectively. The phase noise of the multiphase LO generator is dominated by the first two correctors due to their static phase-correcting operation. Table VI compares the achieved phase-noise performances with those of existing works designed for mobile-TV applications [1], [2]. Certainly, the comparison will be more accurate when the measurement results are available. Since the VCO here is free running, while it is phase locked in existing works, it would only be reasonable to compare the phase noise at 1-MHz offset where the VCO's noise is dominant. Consequently, it can be affirmed that the phase-noise performance of the proposed open-loop multiphase LO generator is comparatively acceptable for wireless applications.

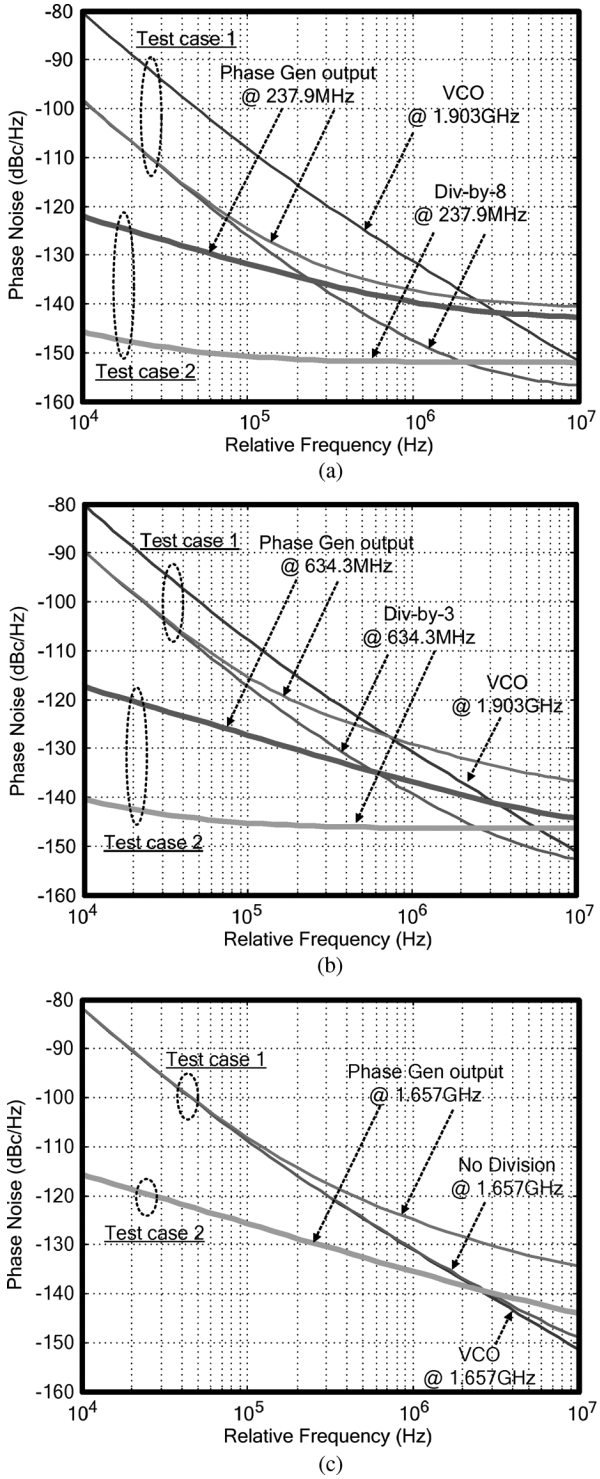

Fig. 21. Phase-noise performances of the quadri-/octave-phase LO generator with noiseless and LC VCO signal sources. (a) VHF-III, (b) UHF, and (c) L-bands (schematic simulations).

IV. CONCLUSION

This paper has described the analysis and design of two open-loop multiphase (quadri and octave) LO generators for wireless applications. The developed circuit mathematical model provides an appropriate insight into circuit dimensioning tradeoffs

TABLE VI
COMPARISON OF PHASE-NOISE PERFORMANCE AT 1-MHZ OFFSET

	VHF-III	UHF	L
[1]	-135 dBc/Hz	-129 dBc/Hz	-123 dBc/Hz
[2]	n/a	n/a	-128 dBc/Hz*
This work#	-137 dBc/Hz	-129 dBc/Hz	-125 dBc/Hz

* estimated by measured 3.8-GHz output signals with ideal div-by-2 operation.
# simulation results.

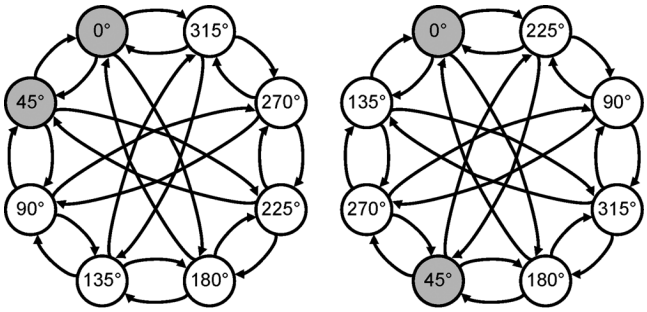

Fig. 22. Phase permutation. (a) Linear-model prediction. (b) Transistor- level simulation.

between frequency range and phase precision. The feasibility of the circuit for wireless applications is demonstrated through the design of two examples in state-of-the-art technologies. Example 1 (octave phase) has been designed in 90-nm CMOS, and it covers the VHF-III and UHF bands with an optimized phase precision within 0.8°. Example 2 was designed and implemented in 65-nm CMOS for use in a 170–1700-MHz full-band mobile-TV tuner. The circuit combines quadri- and octave-phase generation techniques to support image-reject downconversion and image-reject harmonic-reject downconversion, respectively. Extensive schematic and postlayout simulation results accounting for parasitic capacitances and process variations have been provided to demonstrate the robustness of the circuit. The achieved precisions are within 1° (octave phase) and 1.5° (quadri phase) in all process corners. The achieved phase noise of the entire multiphase LO generator using an LC-VCO is comparable with that of existing solutions.

APPENDIX

The linear model applied in the phase corrector has assumed that all inverters operate in the saturation region simultaneously. However, because of the phase difference, the LO signals inside the phase corrector can have a large difference in amplitude. Since certain transistors operate in the triode region featuring a smaller dc gain, it was verified that the phase permutation predicted by the linear model is different from the transistor-level simulation, as shown in Fig. 22. The phase permutation is correct in the linear model, while it is jumped-by-three in the transistor-level simulation (i.e., every adjacent node has 135° phase shift with each other). In order to explain this phenomenon, an eigenvector analysis has been applied. There are eight eigen-

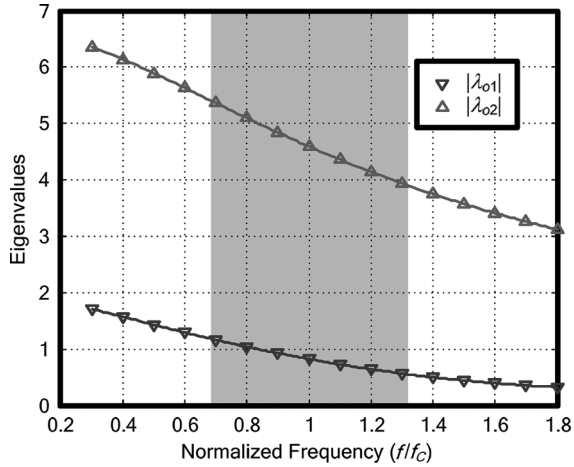

Fig. 23. Two critical eigenvalues of the octave-phase corrector.

pairs [28] of A_o [(17)], but only two are worth considering, which are

$$(\lambda_{o1}, \phi_{o1}) = \begin{pmatrix} 1-(e^{\frac{-j\pi}{4}}+e^{-j\pi})ah - e^{\frac{-j7\pi}{4}}bh \\ \frac{1}{\sqrt{8}}\begin{bmatrix}1 & e^{\frac{-j\pi}{4}} & e^{\frac{-j\pi}{2}} & \cdots & e^{\frac{-j7\pi}{4}}\end{bmatrix}^T \end{pmatrix} \tag{22}$$

and

$$(\lambda_{o2}, \phi_{o2}) = \begin{pmatrix} 1-(e^{\frac{-j3\pi}{4}}+e^{-j\pi})ah - e^{\frac{-j5\pi}{4}}bh \\ \frac{1}{\sqrt{8}}\begin{bmatrix}1 & e^{\frac{-j3\pi}{4}} & e^{\frac{-j3\pi}{2}} & \cdots & e^{\frac{-j5\pi}{4}}\end{bmatrix}^T \end{pmatrix} \tag{23}$$

where λ_{o1} and λ_{o2} are the eigenvalues of A_o, and ϕ_{o1} and ϕ_{o2} are the eigenvectors of A_o. The represented ϕ_{o1} and ϕ_{o2} are two different phase permutations, as shown in Fig. 22(a) and (b), respectively. The gain of each mode depends on the inverse of the corresponding eigenvalue, so the mode with a smaller corresponding eigenvalue is the dominant mode in the linear model. As shown in Fig. 23, $|\lambda_{o1}|$ has a smaller value than $|\lambda_{o2}|$ in the targeted frequency range (as shown in Fig. 10). Thus, the dominant mode is ϕ_{o1} in the linear model. However, due to nonlinear effects, as already highlighted, the dominant mode obtained from the transistor-level simulation is ϕ_{o2}. Nevertheless, this difference of prediction will not induce an error. The transistor-level implementation guarantees that the phase permutation is unique with ϕ_{o2} under all possible test cases.

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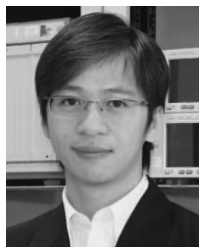

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Rui P. Martins (M'88–SM'99–F'08) was born in April 30, 1957. He received the B.S. (five years), M.S., and Ph.D. degrees as well as the *Habilitation* for Full Professor in electrical engineering and computers from the Department of Electrical and Computer Engineering, Instituto Superior Técnico (IST), Technical University (TU) of Lisbon, Lisbon, Portugal, in 1980, 1985, 1992, and 2001, respectively.

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Prof. Martins was the Founding Chairman of the IEEE Macau Section from 2003 to 2005 and of the IEEE Macau Joint-Chapter on Circuits and Systems/Communications from 2005 to 2008 [*World Chapter of the Year 2009* of the IEEE Circuits and Systems Society (CASS)]. He was the General Chair of the 2008 IEEE Asia-Pacific Conference on Circuits And Systems and was elected as Vice-President for the Region 10 (Asia, Australia, and the Pacific) of CASS for the period of 2009–2010. He is an Associate Editor for the IEEE TRANSACTIONS ON CIRCUITS AND SYSTEMS II—EXPRESS BRIEFS for the period of 2010–2011. He was the recipient of two government decorations: the *Medal of Professional Merit* from the Macao government (Portuguese administration) in 1999 and the *Honorary Title of Value* from the Macao SAR government (Chinese administration) in 2001.